Ring Oscillators for CMOS Process Tuning and Variability Control

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***Abstract*—Test structures utilizing ring oscillators to monitor MOSFET ac characteristics for digital CMOS circuit applications are described. The measurements provide information on the average behavior of sets of a few hundred MOSFETs under high speed switching conditions. The design of the ring oscillators is specifically tailored for process centering and monitoring of variability in circuit performance in the manufacturing line as well as in the product. The delay sensitivity to key MOSFET parameter variations in a variety of ring oscillator designs is studied using a compact model for partially depleted silicon on insulator (PD-SOI) technology, but the analysis is equally valid for conventional bulk Si technology. Examples of hardware data illustrating the use of this methodology are taken primarily from experimental hardware in the 90-nm CMOS technology node in PD-SOI. The design and data analysis techniques described here allow very rapid investigation of the sources of variations in circuit delays.**

***Index Terms*—Circuit sensitivity analysis, CMOS integrated circuits, CMOSFET oscillators, integrated circuit manufacture, integrated circuit modeling, process monitoring.**

I. Introduction

With advances in silicon CMOS technology and scaling of MOSFET channel lengths to 90 nm and below, process induced variations in circuit delays have begun to significantly impact product performance and power. Variations in circuit delays and leakage power of nominally identical structures may occur locally, across chip, across reticle in a multi chip reticle, across wafer, from wafer-to-wafer and from lot-to-lot. In addition, tracking amongst different circuit topologies may also vary in a similar fashion. In a silicon manufacturing line, dc characteristics of single MOSFETs and other structures are monitored on a limited number of sites on a few selected wafers in each lot for tracking and process tuning. These test structures are placed in the scribe line and do not adequately capture all the variations or provide comprehensive insight into their sources. We have developed and introduced a variety of test structures for efficiently extracting delay components and MOSFET parameters (see Table I) from high speed measurements of a collection of circuits in IBM's 90 nm and 65 nm technology nodes [1]. These test structures are of two general forms: ring oscillators and single-shot, pulse-based circuits. This work focuses on ring oscillators and specifically addresses their use in tracking the mean values and variations of circuit performance and of key device parameters. The application of such structures to the diagnosis of sources of variation is also demonstrated. While ring oscillators have been used routinely for many years to determine performance of particular circuit types, we have extended their utility by employing circuit configurations that enable self-consistent determination of key MOSFET parameters at gigahertz frequencies.

TABLE I
Description of MOSFET Parameters

MOSFET Parameter	Description
Lp	Channel Length
Vt	Threshold Voltage
Cg	Gate Capacitance
Cov	Drain/source-to-gate overlap Capacitance
Cj	Drain/source-to-body Capacitance
Cdiff	Drain/Source diffusion Capacitance
Rds	Drain/source series resistance

Ring oscillators can be made up of product representative circuits operating under high-speed conditions much as in an actual product application. Measurements made under such conditions are fundamentally closer to technology applications than standard dc parametric measurements. This is an important consideration in general, but especially for technologies such as PD-SOI or high-k gate dielectric CMOS where dc measurements of MOSFET parameters do not accurately reflect the behavior under high-speed switching conditions because of floating-body and self-heating effects (PD-SOI) or various dielectric relaxation mechanisms in high-k gate dielectric materials. Local statistical fluctuations in device parameters such as threshold voltage, Vt, variations arising from dopant fluctuations, and line edge roughness can introduce significant mismatch in delay and leakage between nominally identical circuits in close physical proximity [2], [3]. With the ring oscillator approach, these random variations are greatly reduced in the analysis by averaging over a few hundred logic gates, giving much more robust mean values than those obtained from individual MOSFETs. Precise determination of effective electrical channel length has become increasingly difficult in technology nodes beyond 90 nm. A ring oscillator based approach enables a power performance representation of a technology in which the channel length itself need not be known to make comprehensive technology assessments. Ring oscillators can be used in conjunction with an on-board

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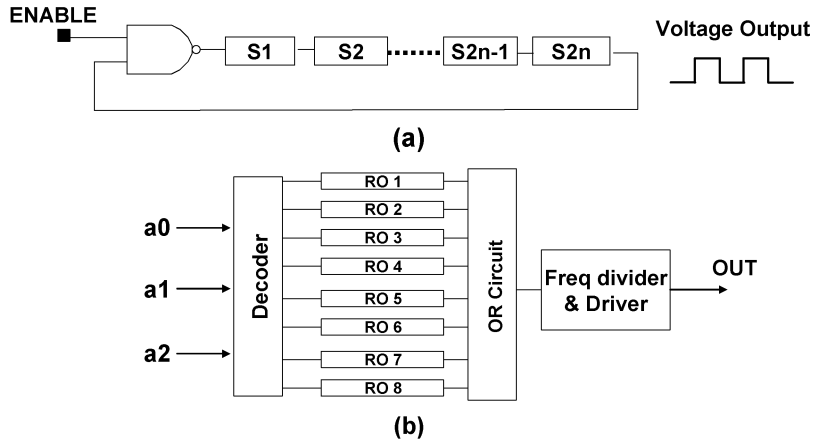

Fig. 1. (a) Ring oscillator circuit with 2n identical stages and a NAND2 gate for enabling the oscillations and (b) scheme for implementing eight ROs with a 3-bit decoder and a common output.

frequency divider to give an output frequency of a few MHz or less, easily measurable with a low-cost frequency counter in a standard parametric measurement setting. Ring oscillator structures testable as early in the process as first level of metal are used for initial technology development as well as technology monitoring in manufacturing. Other ring oscillator structures are embedded within the product chip design itself and can be used to diagnose product and technology performance at wafer final test and in the packaged product.

In this paper, we first describe the design of ring oscillator (RO) structures and the strategy behind those designs. We then present data from experimental hardware to illustrate the use of these structures to evaluate power/performance, to derive MOSFET characteristics, and to illustrate the relationship of circuit performance variations to device parameter variations.

II. Ring Oscillator Design

ROs have been commonly employed for circuit delay measurements. The resistance and capacitance components of a circuit delay can be derived from the measurements of RO frequency, f, and average dc currents drawn (as measured with a current meter at the RO power supply) in the oscillating and quiescent states, IDDA and IDDQ respectively [1]. The delay per stage, D, and capacitance per stage, Cs, in a ring with 2n identical stages and a NAND2 gate are given by

$$\mathrm{D} = \frac{1}{(4\,\mathrm{mnf})}, \quad 2\mathrm{n} \gg 1 \tag{1a}$$

$$\mathrm{Cs} = \frac{2\mathrm{D}(\mathrm{IDDA} - \mathrm{IDDQ})}{\mathrm{VDD}} \tag{1b}$$

where each stage switches twice during a complete cycle, m is the divide by factor in the output and VDD is the RO power supply voltage. A more precise determination of the delay per stage can be obtained by using a circuit simulation based correction for the NAND2 delay. This correction is not necessary in comparing hardware results to actual model predictions as the simulations are carried out for the full RO circuit including the NAND2. The delay per stage is also expressed in terms of the switching resistance, Rsw, and Cs,

$$\mathrm{D} = \mathrm{Rsw}\ \mathrm{Cs}. \tag{2}$$

Here Rsw is a measure of the current drive capability and in turn represents the MOSFET drain-source current-voltage, Ids-Vds, characteristics of the MOSFETs comprising the CMOS logic gates under their respective voltage bias conditions.

The circuit schematic of a ring oscillator with 2n identical stages and a NAND2 gate to enable the oscillations is shown in Fig. 1(a). Any number of product representative ring oscillators may be placed in a single macro as illustrated in Fig. 1(b) for eight ROs. A p bit decoder sets the enable signal high to select any one of 2^p ROs and the outputs of all the ROs are "OR'ed" together and fed to a frequency divider circuit and then to an off-chip driver. The ROs may be placed in close physical proximity in a compact macro or spread across the product. Because of constraints on space and number of available I/Os there is an incentive to share power supply, VDD terminals among multiple ROs. Typically all ROs in a macro share a common ground terminal, GND. If the VDD terminal of each RO is isolated, the IDDQ of an individual RO can be measured independently. Alternatively, several ROs may share a common VDD terminal and the measured IDDQ represents the sum of the IDDQs of all ROs in the set. The Cs of each RO can still be determined by using the measured IDDQ as the background leakage current. In these two cases, the peripheral circuits must have an independent power source. For ROs placed on the product, the power supply source is shared with all other circuits and the IDDQ values of the individual ROs cannot be measured. Information on capacitance changes and parameter variations is obtained by tracking RO delays to a reference RO delay and comparing to model predictions.

Basic structures for measuring capacitance using a set of two ROs are depicted in Fig. 2(a) with a reference inverter stage and in Fig. 2(b) with an inverter stage having an additional capacitive load CL, in this case a gate capacitance. The value of CL is estimated as the difference in the values of Cs of the two ROs. The physical size and the wiring of the stages are identical as

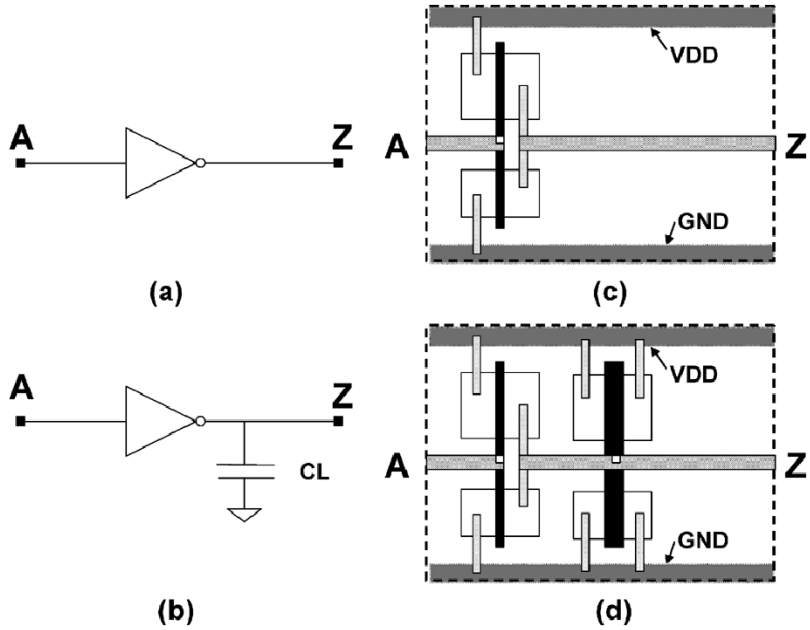

Fig. 2. Circuit schematic and physical layout of a RO stage for (a) inverter $(\mathrm{FO} = 1)$ reference and (b) inverter with a MOSFET gate load, CL.

shown in Fig. 2(c) and (d) so that the parasitic capacitances and resistances associated with the wires are eliminated by using this subtraction technique. Capacitance differences <1 fF are easily resolved. CL may physically correspond to gate capacitance, Cg, wire capacitance, Cw, diffusion capacitance, Cdiff, or overlap and junction capacitance, Cov and Cj respectively. It is preferable to make these measurements at subnominal VDD so that the short-circuit current through the CMOS gate does not significantly influence the capacitance estimation [4].

For MOSFET dc parameters, the subthreshold leakage current, Ioff, and gate leakage current, Ig, are also determined by using a subtraction technique. Ig is estimated from the difference in IDDQ of the stages in Fig. 2(a) and (b). The individual NFET and PFET Ig contributions can be separated using ROs with only NFET or only PFET loads. Knowing the values of Ig, the separate NFET and PFET Ioff values can be determined from the reference RO along with one additional inverter RO having a different PFET width. The measurement of capacitance, leakage and frequency provides the basis for estimating power (switching and leakage) and performance of a product without a direct knowledge of effective channel length.

The value of Rsw for a logic gate is a measure of its current drive capability during switching. The Rsw and capacitances of a CMOS logic gate can be estimated from three ROs, all with the same logic gate but driving three different fanout, FO, loads with $\mathrm{FO} = 1$, $\mathrm{FO} = 3$, and $\mathrm{FO} = 1$ plus a known capacitive load (CL), using the expressions below [1], [5]:

$$\mathrm{D1} = \mathrm{Rsw}(\mathrm{Cin} + \mathrm{Cout}) \tag{3a}$$

$$\mathrm{D2} = \mathrm{Rsw}(3\mathrm{Cin} + \mathrm{Cout}) \tag{3b}$$

$$\mathrm{D3} = \mathrm{Rsw}(\mathrm{Cin} + \mathrm{Cout} + \mathrm{CL}). \tag{3c}$$

Here Cin is the input capacitance of the driving gate and Cout is its output capacitance. Cin is the gate oxide capacitance along with the overlap capacitance, Cov. Cout is a combination of diffusion and junction capacitance along with some fraction of Cin. In a specific inverter design, Rsw, Cin, and Cout are averaged over NFET and PFET. The influence of each FET type can be enhanced by designing gates with different PFET and NFET widths, Wp and Wn, respectively.

For wire capacitance determination of different metal layers with varying metal line widths and spaces, ROs with identical driving inverter stages and different metal loadings are used. In all these cases, the wire resistance, Rw, is negligible compared to the Rsw of the driving inverter $(\mathrm{Rsw} \gg \mathrm{Rw})$. The effect of wire resistance, Rw, is determined by designing the RO stage with a very wide inverter and a long wire such that the inverter Rsw is less than Rw.

Different Ids-Vds trajectories vary with logic gate type and can be sampled by appropriately designing the logic gates [1], [5]. This method is in fact more relevant to studying MOSFET behavior in actual circuit applications than the traditional measurement of a few discrete points on Ids-Vds plots. In the case of stacked gates (NANDs and NORs), the NFET and PFET device widths are kept constant as the stack height is increased. The change in Rsw with increasing number of NFETs in NAND gates gives a measure of the linear source-drain resistance of an NFET. While Cin and the load are maintained constant $(\mathrm{Wp} + \mathrm{Wn} = \mathrm{constant})$, change in Cs, which now directly relates to Cout, as a function of NFET stack height isolates the NFET diffusion capacitance. The source-drain resistance and the diffusion capacitance of the PFET can be similarly obtained from a set of ROs comprising NOR gates with different PFET stack heights and a constant total width $(\mathrm{Wp} + \mathrm{Wn})$.

The value of Rsw for a gate and subsequently its delay vary with Vt/VDD. The change in delay with VDD gives a measure of Vt but the influence of changes in NFET and PFET Vts cannot be separated easily. However, delays and Rsw values of stages comprising inverters in series with single ended NFET or PFET

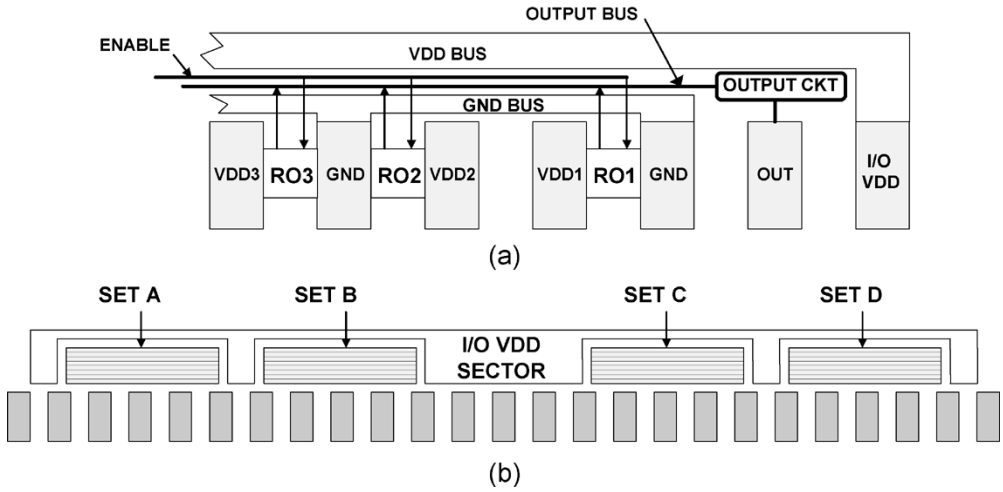

Fig. 3. Physical structure of RO macros with 25 I/Os: (a) three of 13 ROs with independent VDDs for test at M1 and (b) thirty-two ROs (four sets A, B, C, and D, each eight ROs high) for test at M3, with the decoder and output circuitry including a distributed OR function and buffers, frequency divider, and off-chip driver, all located in the I/O VDD sector. Each set of eight ROs is powered independently. Both macros are 2.5 mm across and $<200\ \mu$m high.

passgates are very sensitive to the Vt of the passgate as long as the passgate width is narrow compared to the inverter, and the delay is dominated by the Rsw of the passgate [1], [4]. Changes in NFET and PFET Vts can thus be monitored independently with passgate ROs.

A common reference RO may serve a number of other nearby ROs as long as stage width and wiring are kept identical. The stages are tiled together to form the RO facilitating design changes in a hierarchical fashion. The ROs have 25, 51, or 101 stages ($\mathrm{n} = 12$, 25, or 50) and CMOS logic gates comprise multifingered MOSFETs. The measurements, averaged over a few hundred MOSFETs, provide an insight into systematic variations in circuit and MOSFET parameters, the impact of local statistical variations being minimized.

Based on power supply configuration we have designed three different categories of RO test structures. The first, with an independent VDD for each RO, is used for the most direct evaluation of MOSFET and parasitic parameters from the known delay, IDDQ and Cs of each RO. An example physical layout for this type of macro with 25 I/O pads is shown in Fig. 3(a). This particular design requires only the first metal layer (M1) for wiring. Crossovers are laid out with local interconnect, gate polysilicon layer, PC, or Si diffusion layer. Each RO is placed between a VDD and GND pad with a low resistance power distribution system taking the form of two interdigitated combs.

The second category of RO test structures in which a number of ROs share a common VDD for reducing the number of I/Os per RO. An example physical layout of such a design is shown in Fig. 3(b). This macro has four sets of eight ROs, A, B, C, and D. Each set has a common VDD with a product representative power grid. The information derived from this macro configuration is restricted to delay, Cs and Rsw for individual rings along with IDDQ of each set. The aspect ratio of these first two categories is well suited for placement in the scribe line.

In the third category of RO test structures, ROs are powered by the power distribution system of the entire product chip. Such ROs may be distributed across the surface of the chip and may be an integral part of the chip design itself. In this case, only the frequency of each RO is measured after completion of the full process or at system level at any time during the lifetime of the product. This implementation is particularly useful for observing aging phenomenon due to NBTI and hot-carrier effects during the lifetime of a product under actual use conditions. Information on the capacitances and MOSFET parameters is derived by using a calibrated capacitance in the ROs and by monitoring the tracking of each circuit type with respect to a reference RO. The set of these ROs are designed to enhance the delay sensitivity to different MOSFET parameters such as Vt, Rds and Cov in different ROs. The delays of these ROs normalized to the model predictions are compared to the normalized delay of a reference RO with Lp as a variable. The delay tracking among ROs provide a rapid evaluation of device parameter variation in the hardware.

III. Mesurements and Data Analysis

The concepts described above are illustrated with examples derived from SPICE simulations using a generic BSIM model for the 90-nm PD-SOI technology node. Corresponding results are shown from hardware data on several experimental lots for the same technology. Each point of the hardware data is randomly selected from measurements made on a single reticle location on specific sites on a wafer. The hardware data captures the trends shown by the models although no attempt is made here to do a true model-to-hardware correlation. In a manufacturing line, this type of analysis and offsets between model and hardware provide direct information for process and device monitoring and tuning on an on-going basis. For a more detailed understanding of the MOSFET behavior, standard dc characterization is carried out and correlated to the ac performance.

Fig. 4(a) shows the simulated IDDQ versus delay of a reference inverter RO and an inverter RO with additional load, CL. Here channel length, Lp, is varied to get a range of IDDQ and delay, where the delay decreases with decrease in Lp. The increase in IDDQ with decrease in delay arises primarily from the decrease in Vt at shorter Lp. The difference in IDDQ between

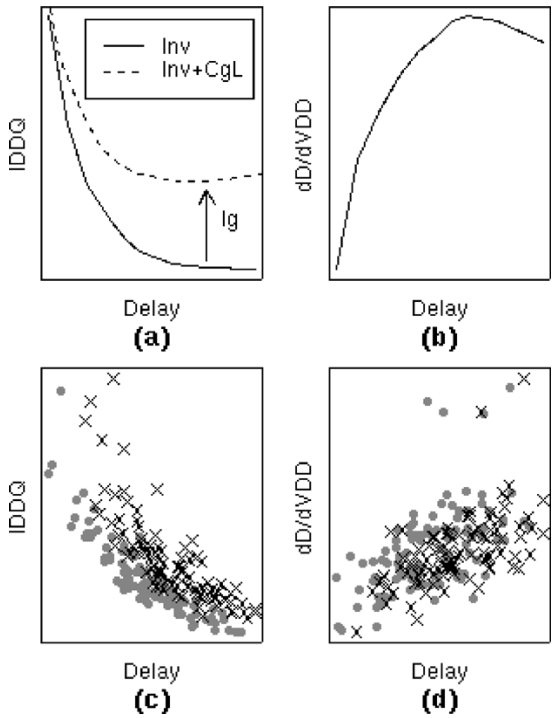

Fig. 4. Simulated results showing (a) IDDQ versus delay of reference and gate loaded ROs, (b) dD/dVDD versus delay and hardware data from two lots showing (c) IDDQ versus delay and (d) dD/dVDD versus delay.

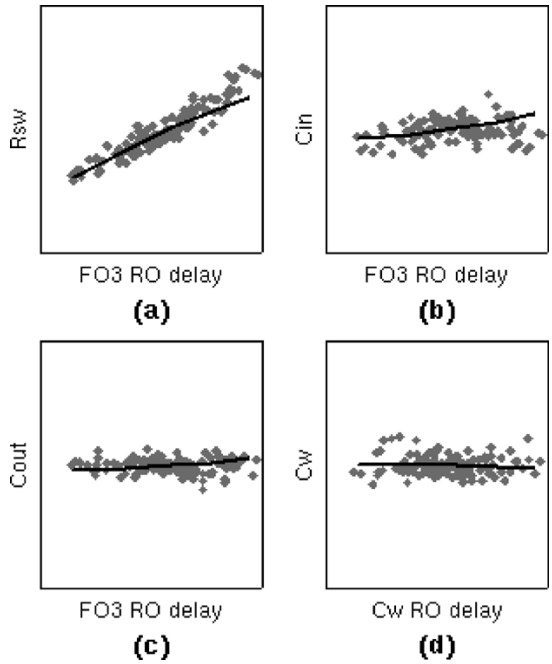

Fig. 5. Hardware data and simulations (solid lines) showing inverter (a) Rsw, (b) Cin, (c) Cout as a function of FO3 inverter delay, and (d) Cw as a function of wire loaded RO delay.

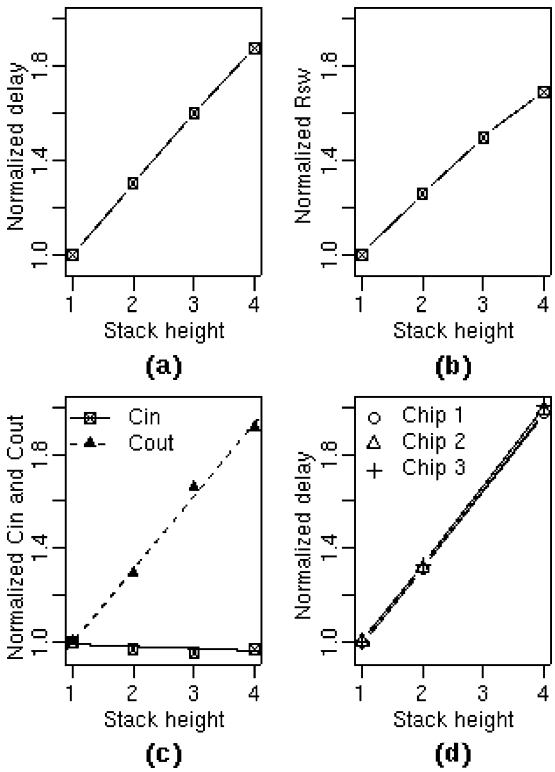

Fig. 6. Simulated results showing (a) delay (b) Rsw, (c) Cin, and Cout as a function of NFET stack height in an inverter and NAND gates, and (d) hardware data showing delay versus stack height on three chips.

the two ROs at longer delays and for a constant Vt gives a measure of the gate leakage, Ig. In Fig. 4(b), the change in delay with VDD is plotted against the delay. The decrease in dD/dVDD for smaller delays corresponds to a lower Vt and corresponding increase in IDDQ. In Fig. 4(c) and (d), hardware data for IDDQ versus delay and dD/dVDD in the short Lp range is shown for two different lots. It can be observed that higher IDDQ roll-up corresponds to lower dD/dVDD or in turn lower Vt and that the spread in IDDQ at a fixed delay is influenced by Vt variations in the hardware.

In Fig. 5(a)–(c), the hardware data for Rsw, Cin and Cout of an inverter are shown as a function of delay. The RO delay variations in the hardware are primarily related to variations in Lp. Rsw increases linearly with delay, Cout and Cwire are constant and Cin gradually decreases as Lp is reduced. To a first order, trends in the hardware data are well correlated to the model predictions indicated by a solid line using Lp as the variable. Fig. 5(d) shows Cw as a function of the delay for RO comprising an inverter driving a capacitive wire load.

Fig. 6(a)–(c) shows model predictions of delay, Rsw, Cin and Cout as a function of stack height for an inverter and top input switching NAND gates. A stack height of one corresponds to an inverter and all gates have the same Wp and Wn. The delay and Rsw vary linearly with stack height, the increase in Rsw being a measure of the linear resistance contribution of the NFETs in the stack. Similarly, Cout increases with stack height as the diffusion and junction capacitance contributions of each additional NFET in the stack are added. Cin remains unchanged with stack height corresponding to a constant $\mathrm{Wp} + \mathrm{Wn}$. Fig. 6(d) shows hardware examples of delay versus stack height for a set of inverter and NAND gates for three chips.

The largest independent contributing factor to change in circuit delay for static gates is Lp. If the hardware represents the model correctly, the delays of all static gates will track with each other according to model predictions as Lp is varied.

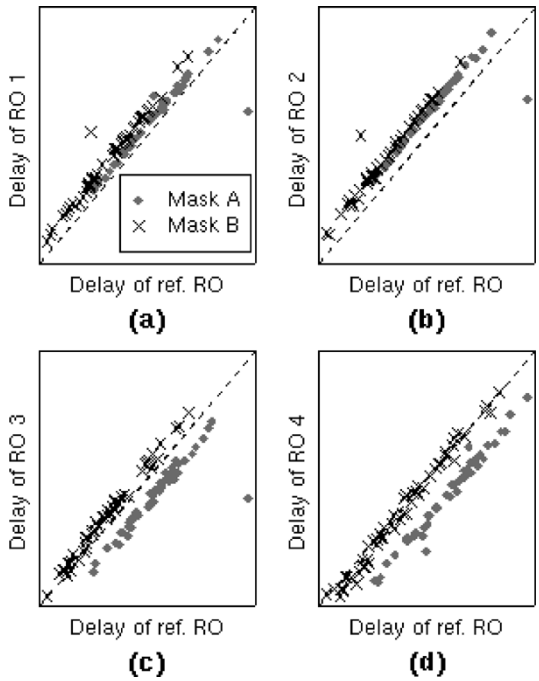

Fig. 7. Hardware data employing two different PC masks and comparing delays of four schematically identical ROs of different PC pitch with delay of a reference RO. Dashed lines show 1:1 correspondence.

This also assures that the product frequency can be adjusted by simply changing the lithographic process and adjusting Lp. Other sources of variations such as physical topology, Vt, Rds, Cov, and parasitic resistances and capacitances may cause deviations from expected circuit delays. These variations could be local, across wafer or across hardware of different vintage. RO designs and data analysis techniques to detect these sources of variations are described below.

The physical layout rules defined by the silicon manufacturing industry for a given technology node allow some flexibility in layout styles. Each product may employ several different layout styles for area efficiency and ease of wiring the circuits. Some of these differences may impact the performance of the circuit because of variations in parasitic resistances and capacitances as well as variations in stress induced mobility of the MOSFETs. Local pattern density variations may also impact the final physical dimensions of the layers from process induced variations in etching and chemical–mechanical polishing. Other sources of variations may arise from Optical Proximity Correction (OPC) algorithms used in generating the masks. RO test structures provide a direct way of evaluating tradeoffs amongst various layout styles used in a product by comparing the average performance of a representative set of gates of each layout style. This application is illustrated in Fig. 7 where the stage delays of four ROs are compared with a reference RO. The ROs are identical in all respects except for local polysilicon, PC, gate density and the data shown are from hardware fabricated with two different mask sets. Here deviations from the 1:1 correspondence line are easily observed. For example, mask A has comparable delays with mask B for RO1 and RO2 but smaller delays for RO3 and RO4.

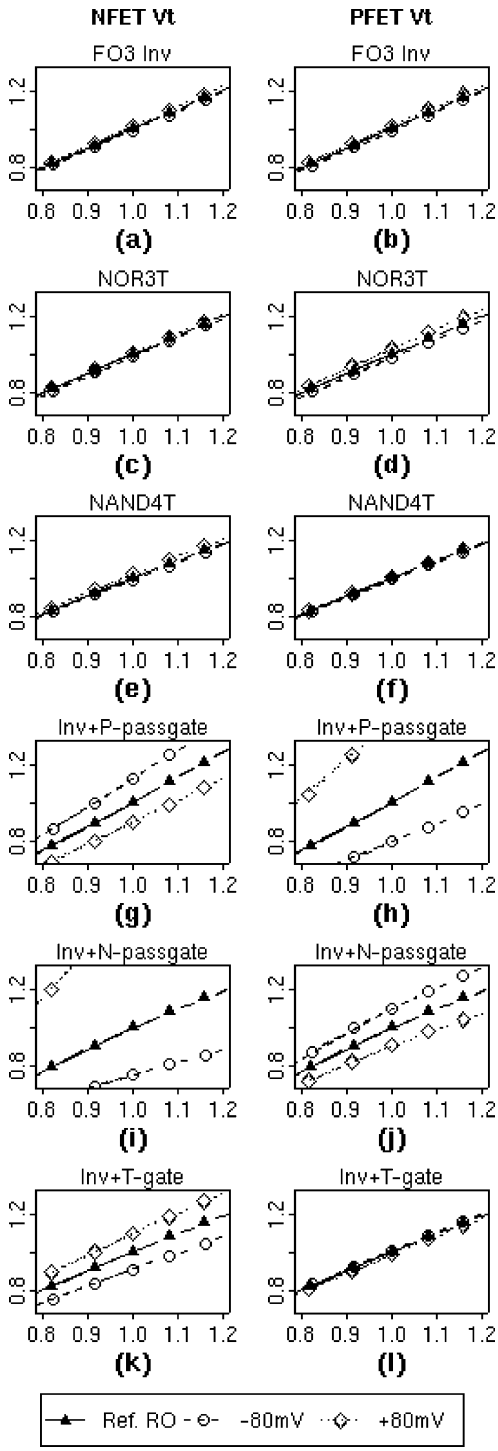

Fig. 8. Simulated results showing delay tracking of different circuit types over a range of Lp and nominal Vt with a reference inverter (solid line). The dashed lines show the delay with change in NFET Vt of $+/-80$ mV and change in PFET Vt of $+/-80$ mV. Horizontal axes are normalized reference inverter delays and vertical axes are normalized delays of indicated gate type.

The variations in Vt can be picked up by tracking the delay of different circuit types with respect to the delay of a reference circuit. Sensitivities of circuit delays to Lp variations using SPICE simulations are shown in Fig. 8(a)–(l). The reference circuit selected here is an inverter with a gate load. The circuit types investigated include FO3 inverter, three-input NORwith the

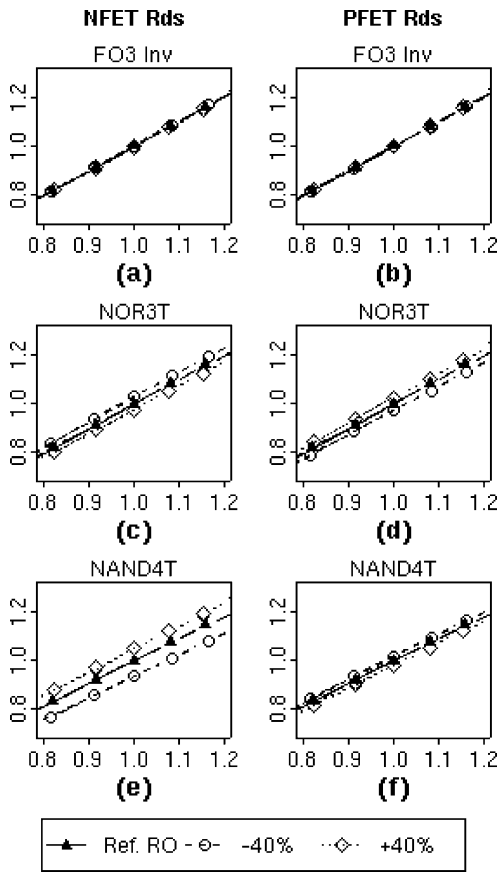

Fig. 9. Simulated results showing delay tracking of different circuit types over a range of Lp and nominal NFET Rds and PFET Rds with a reference inverter (solid line). The dashed lines show the delay with change in Rds of $+/-40\%$. Axes are as described in Fig. 8.

top input switching (NOR3T), four-input NAND with top input switching (NAND4T), inverter driving a PFET passgate (Inv + P-passgate), inverter driving an NFET passgate (Inv+N-passgate) and inverter driving a transmission gate (Inv+T-gate) [1], [4], [5]. The x axis in all plots (a) through (l) is the normalized delay of the reference inverter. The y axis in each plot is the normalized delay of the indicated circuit type. The solid line corresponds to the normalized circuit delays with all circuit types including the reference inverter having nominal NFET and PFET Vts. The dashed lines correspond to an NFET Vt change by $+/-80$ mV in the left column and PFET Vt change by $+/-80$ mV in the right column for all circuits including the reference. If with change in Vt, the circuit delays track perfectly with the reference inverter, the data points will continue to lie on the solid line. Any miss-tracking in the circuit delay with respect to reference inverter will cause a shift up for larger delay and a shift down for smaller delay from the solid line. This methodology for representing relative circuit performance variation with Vt is directly applicable to comparison with hardware data rendered in a similar fashion. As far as tracking is concerned, a precise determination of Lp and Vts is not required. Looking at Fig. 8(a)–(f) we observe that inverters, NANDs and NORs all track together with a uniform shift in Vt. Passgates, on the other hand, show a very different behavior. The N-passgate delay is a strong function of NFET Vt and P- passgate is a strong function of PFET Vt, both N-passgate and P-passgate are much more sensitive to NFET and PFET Vt changes than are inverters. The PFET and NFET widths in the T-gate are equal and its delay is dominated by the NFET. Hence, its delay shows a larger sensitivity to NFET Vt than to PFET Vt but the range of variation is still much less than that of the N-passgate circuit.

The approach described for analyzing the impact of Vt variations on circuit delay can be generalized to any parameter variation. As further examples in Fig. 9, we show the normalized comparison of delay variations arising from variations in NFET Rds and PFET Rds. The reduced sets of circuits shown in Fig. 9 include FO3 inverter, NOR3T and NAND4T. The NAND4T delay is more sensitive to NFET Rds than the FO3 inverter or NOR3T because its Rsw is influenced by the series resistance of the NFETs in the stack. This effect is present but less pronounced in the NOR3T because of its reduced stack height.

In Fig. 10, hardware data from three different experimental lots are shown for the same circuit types as in Fig. 8. The data is represented in the same format as in Fig. 8 with the normalized delay of a reference inverter on the horizontal axis and normalized delay of the indicated circuit type on the vertical axis. The solid diagonal line in each plot is the 1:1 correspondence line. For data points below this line, the circuits are faster than nominal expectation and for data points above the line the circuits are slower than nominal expectation. The three lots show different characteristics. In lot 1, the N-passgate is somewhat faster indicating a lower NFET Vt. In lot 2, the N-passgate is considerably faster while the P-passgate is slower. The lower NFET Vt reduces the T-gate delay and the higher PFET Vt slows the NOR3T circuit relative to lot 1. In lot 3, both the N and P-passgates show a bimodal behavior which is characteristic of a process split. In this case, the P-passgate circuit is much faster and this is also reflected in the NOR3T circuit delay. In all three lots, the Vts are significantly shifted from nominal and dominate the deviation from the expected values. To get the precise shift in Vts the model parameters can be changed to get a better fit to the hardware.

This type of analysis can be extended to a larger selection of circuit topologies to extract information on other MOSFET parameters and parasitics. In addition to standard CMOS gates, special designs can be included that accentuate the sensitivity to specific parameters. Model predictions for this expanded set of ROs can be directly compared to hardware data and multiple sources of variations identified in an extension of the methodology described in the discussion of Figs. 8–10.

IV. Summary

The RO test structures described here provide a rapid means of evaluating the effect of variations in key MOSFET parameters on switching delays and both active and leakage power of CMOS circuits. The measurements represent an average over sets of a few hundred identically designed MOSFETs and are not affected by random statistical fluctuations in the parameters of isolated single MOSFETs traditionally used for process monitoring. Using the RO design methodology outlined in this work, the sources of systematic components of variability in circuit delays across product, across wafer and across hardware vintage as well as with different physical layout styles can be readily

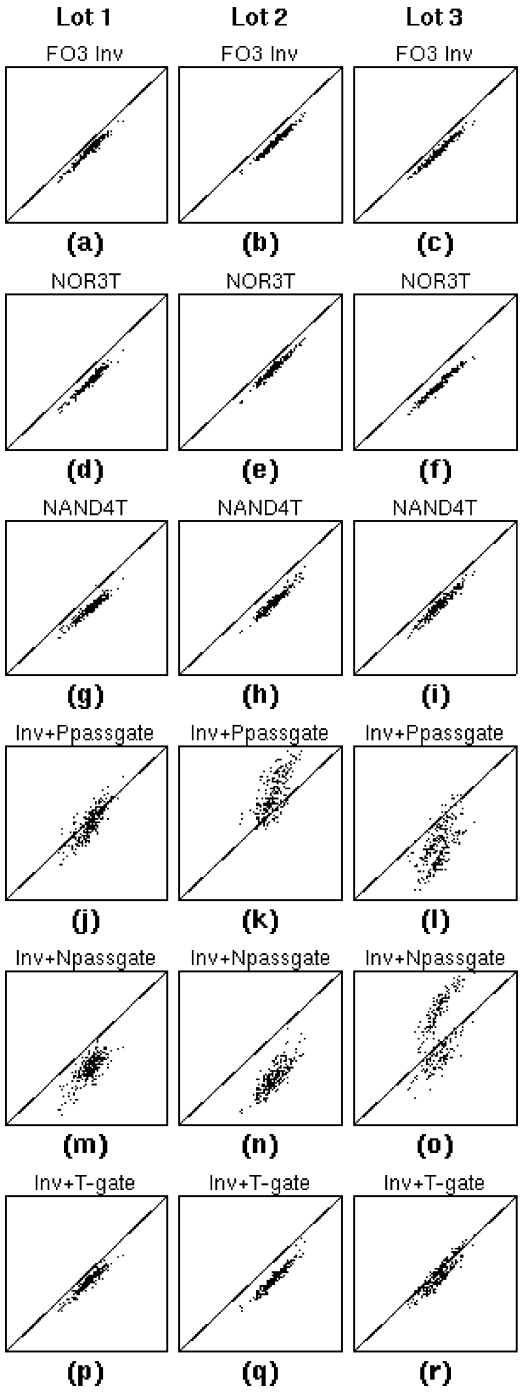

Fig. 10. Hardware data from three different lots showing tracking of normalized delays of different indicated circuit types with normalized delay of a reference inverter RO. The data is shown in the same format as Fig. 8.

identified. These designs are placed in the scribe line for detailed analysis of MOSFETs as well as being integrated into the product itself. A methodology for comparing model predictions of normalized circuit delays with the hardware data is described and example results are presented.

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