

# Reliability and Yield: a Joint Defect-oriented Approach

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## Abstract

*We present a model for computing the probability of a parametric failure due to a spot defect. The analysis is based on electromigration in conductors under unidirectional current stress. Analytical solution is given for simple layout and simulations for a more complicated case. Then we show that in some cases electromigration-dependent parametric defects can make a significant contribution to the total yield estimation.*

## 1 Introduction

### 1.1 Reliability and Electromigration

With the huge advance in technology, reliability of VLSI devices demands greater efforts from both academia and industry. Many factors affect the reliability, among them are: thermal and mechanical strains, radiation, electromigration, and more. The latter is caused by excessive current in metal wires. Electrons at high current have enough energy to drive out lattice ions from their locations. Therefore a void grows in a wire, which finally disconnects the two metal parts.

International Technology Roadmap for Semiconductors (ITRS) predicts increasing of electromigration importance: “Electromigration . . . will become a more limiting factor . . . It must be addressed together with thermal/mechanical reliability modeling. Electromigration may become a limiting factor as the current per unit area increases.” [1].

### 1.2 Scope of this study

In this paper we shall introduce a model for reliability in terms of a special kind of yield problem.

Usually, the term *yield* can be defined as the ratio of the number of items that are usable after completion of production to number at start of production that have the potential to be usable [2]. The term *usable* is usually interpreted as complying to all logical specifications, and such yield is called *catastrophic yield*.

Wagner and Koren in [3] discuss the *parametric yield*, in which the question is: “How many chips will have an acceptable performance?”. The term *acceptable performance* may

have different interpretations, e.g. frequency, power consumption, Mean Time To Failure (MTTF), supply voltage, ambient temperature, etc. In their paper they develop an approach to estimate the frequency dependant yield of long interconnect lines. In this manuscript we shall focus on *electromigration-dependent parametric yield* (EPY), where one is concerned about the number of chips that will survive electromigration for a given period of time.

EPY is a function of layout geometry, the *desired* MTTF, and current flow data, along with working temperature, metal properties and some other process data. The proposed analysis attempts to evaluate the projected ratio of chips complying MTTF target to all the chips that found to be “usable” as defined above.

### 1.3 Previous Works

Catastrophic yield is being investigated for at least 30 years. There are many approaches to evaluate the yield. Among them:

- Random defects generation — Monte Carlo method [4].
- Geometric methods. These include Voronoi diagrams , shape expansion, scan-line method, the Ring theorem method, and others [5, 6, 7].

Non-catastrophic defects have been investigated before too. Allan and Walton in [8] define soft faults as those generated by defects that do not connect separate electrical nodes but reduce the distance between them (or reduce the width of a wire but do not cause an open); they show that extra material soft faults may result in device failure due to eventual dielectric breakdown, and apply the EYE tool to estimate the yield considering those faults. However, the algorithm developed in [8] does not simply apply to electromigration-dependent yield because it does not consider the different currents in different wires.

Number of works, summarized in [9] use catastrophic yield data and statistics about process at waferfab to assess EFR — Early Failure Rate — a measure of reliability. The works do not connect the “Reliability Defect Density” to the mechanisms that jeopardize the reliability.

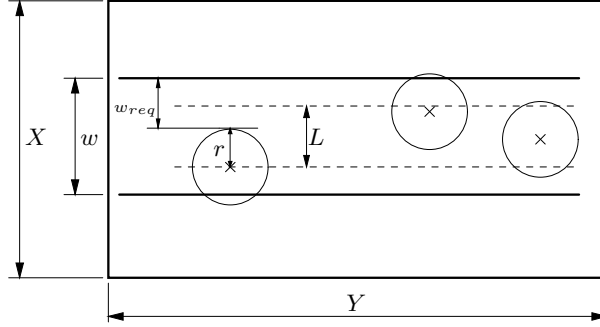
Wagner and Koren in [3] analyze the effect of soft defects on frequency characteristics on long interconnect lines. They derive frequency-dependent critical area based on transmission line model of such wires.

### 1.4 This Work

EPY, developed in this paper, shows the yield for a given target MTTF, considering electromigration. In Section 2 the analytical treatment of EPY is presented for a simple wire; Section 3 deals with practical solution for finding EPY and includes a brief discussion about simulation results; and the Summary shortly recaps the main points of this work.

## 2 Analysis

The probability of spatial defect depends on its location and size. Figures 1 and 2 show a pattern consisting of a single metal wire of width  $w$  much less than its length  $Y$ , deposited on an insulating substrate of width  $X$ . An imperfection in photo mask or photoresist, or contamination can result in the wire be partially or completely broken. If the wire is



**Figure 1. A single wire of width  $w$  in the die of size  $X$ ; with 3 defects of radius  $r$ . The critical interval will be a single strip only if  $r \leq \frac{w}{2}$ .**

completely broken, such defect is called *fatal*, and is well studied [10]. In this section we study defects that cause a partially broken pattern, and calculate  $f(w)$ , the MTTF of a single wire. Among other deficiencies wire width reduction causes growth of current density, which, in turn, leads to MTTF degradation due to electromigration.

Let  $w_{req}$  be the minimal width of wire, such that for a given constant current, its MTTF is at least  $\tau$ . For a defect to become *MTTF-parametric fault* with parameter  $\tau$ , it should fall so that the remaining part of the wire has the width at most  $w_{req}$ .

We answer the following question: Where are the loci of defects that cause the MTTF-parametric fault with parameter  $\tau$ ? Answering the question requires considering two alternative cases, which are presented in Sec. 2.3 and 2.4. Sec. 2.1 and 2.2 give a required background.

## 2.1 Defects size distribution

The defect size probability distribution  $S(r)$  is well-studied during last three decades. It is accepted to be

$$S(r) = \begin{cases} c_q r^q & 0 \leq r \leq r_0; \\ c_p r^{-p} & r_0 \leq r \leq r_M, \end{cases} \quad (1)$$

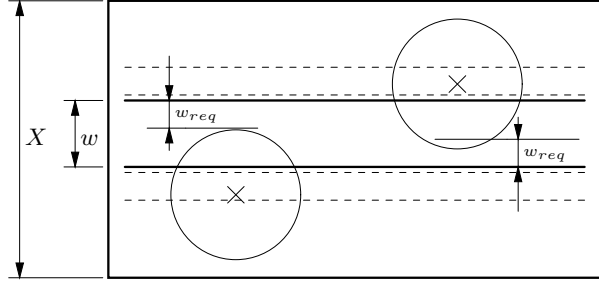
where  $r_0$  is the defect radius at which the density function peaks,  $r_M$  is the maximum size defect expected to occur,  $q \approx 1$ ,  $p \approx 3$ ,  $c_q$  and  $c_p$  are constants such that  $S(r)$  is continuous at  $r_0$  and  $\int_0^{r_M} S(r) dr = 1$  (see [11]). It can be shown that  $r_0 \ll r_M$  (actually,  $r_M \rightarrow \infty$ ),  $q = 1$ , and  $p = 3$  yield

$$\begin{aligned} c_q &\approx \frac{1}{r_0^2} \\ c_p &\approx r_0^2. \end{aligned}$$

## 2.2 MTTF Versus Wire Width

Let us now calculate  $f(w)$ , the MTTF of a single wire of width  $w$ . Black in [12] develops the following equation:

$$\frac{wd}{MTTF} = AJ^2 e^{-\frac{\phi}{kT}},$$



**Figure 2. Two defects greater than wire width  $w$ . The critical interval is split into two strips.**

where

$w$	wire width,
$d$	wire thickness,
$MTTF$	mean time to failure in the wire,
$J$	current density,
$A$	constant embodying physical metal properties,
$\phi$	activation energy,
$k$	Boltzmann's constant,
$T$	wire temperature.

Assuming current  $I$  to be flowing through the wire, we get MTTF as a function of wire width provided all other parameters are constant:

$$MTTF = f(w) = \frac{wd}{AJ^2 e^{-\frac{\phi}{kT}}} = \frac{wd}{A \frac{I^2}{w^2 d^2} e^{-\frac{\phi}{kT}}} = \left( \frac{d^3}{AI^2 e^{-\frac{\phi}{kT}}} \right) \cdot w^3.$$

Defining

$$C \equiv \frac{d^3}{AI^2 e^{-\frac{\phi}{kT}}}$$

we get the following equation:

$$f(w) = C \cdot w^3. \quad (3)$$

It would be useful to express the minimal width required for wire to survive at least  $t$  hours:

$$f^{-1}(t) = \sqrt[3]{t/C}. \quad (4)$$

### 2.3 Small Defects

In this subsection we deal with relatively small radii of defects,  $r \leq \frac{W}{2}$ . Let  $L$  be the critical interval within which the defect must fall in order to cause a parametric fault, i.e., the wire would be operational, but is expected to fail after some time  $\tau$  due to electromigration.  $L$  designates the length of the loci of defects centers that cause the desired MTTF reduction to at most  $\tau$ , while  $w_{req} = f^{-1}(\tau)$ .

Summation of lengths leads to the following equations:

$$\begin{aligned} w &= w_{req} + r + \frac{w - L}{2} \\ L &= 2w_{req} + 2r - w. \end{aligned}$$

The MTTF-parametric fault with radius  $r$  will appear with probability equal to the ratio of  $L$  to the total width  $X$  on which the fault can fall.

$$prob_1(t \leq \tau | r) = \frac{2f^{-1}(\tau) + 2r - w}{X}$$

As said, the wire's remaining width should be at least  $w_{req} = f^{-1}(\tau)$ . Therefore the defects with radius less than  $\frac{w-w_{req}}{2}$  do not contribute MTTF-parametric fault. The *average electromigration-dependent parametric fault probability* (or EP fault probability) for all defects may be obtained by integrating  $prob_1$  multiplied by the fractional number of defects with radius  $r$  over radii sizes

$$prob_1(t \leq \tau) = \int_{\frac{w-f^{-1}(\tau)}{2}}^{\frac{w}{2}} \frac{2f^{-1}(\tau) + 2r - w}{X} \cdot S(r) dr. \quad (6)$$

## 2.4 Big Defects

Now we have to treat another case, where the defect's radius is greater than half the wire's width ( $r \geq \frac{w}{2}$ ). In this case, the critical area, in which the defect must fall in order to cause parametric fault but not catastrophic fault, is built up of two strips each one of height  $w_{req}$  (see Figure 2). Therefore we get

$$\begin{aligned} L &= 2w_{req} \\ prob_2(t \leq \tau | r) &= \frac{2f^{-1}(\tau)}{X}, \end{aligned}$$

and finally

$$prob_2(t \leq \tau) = \int_{\frac{w}{2}}^{\infty} \frac{2f^{-1}(\tau)}{X} \cdot S(r) dr. \quad (7)$$

Actually, the upper limit of integration in the last equation should be finite, since defect size is bounded by the die size. Eq. 1 shows that the likelihood of defects bigger than die is very small, therefore we disregard them. Details regarding bounded and unbounded critical area may be found in [13].

## 2.5 Average Electromigration-dependent Parametric Fault Probability

Since the Equations 6 and 7 are mutually exclusive, the total probability is the sum of the two probabilities:

$$prob(t \leq \tau) = prob_1(t \leq \tau) + prob_2(t \leq \tau). \quad (8)$$

As shown in Sec. 2.1,  $S(r)$  is defined differently in two intervals. Hence, if  $\frac{w}{2} \leq r_0$ ,

$$\begin{aligned} prob(t \leq \tau) &= \int_{\frac{w-f^{-1}(\tau)}{2}}^{\frac{w}{2}} \frac{2f^{-1}(\tau) + 2r - w}{X} \cdot c_q r dr + \\ &+ \int_{\frac{w}{2}}^{r_0} \frac{2f^{-1}(\tau)}{X} \cdot c_q r dr + \int_{r_0}^{\infty} \frac{2f^{-1}(\tau)}{X} \cdot \frac{c_p}{r^3} dr, \end{aligned}$$

which for  $c_q = 1/r_0^2$ ,  $c_p = r_0^2$  yields

$$\begin{aligned} \text{prob}(t \leq \tau) &= \int_{\frac{w-f^{-1}(\tau)}{2}}^{\frac{w}{2}} \frac{2f^{-1}(\tau) + 2r - w}{Xr_0^2} r dr + \\ &+ \int_{\frac{w}{2}}^{r_0} \frac{2f^{-1}(\tau)r dr}{Xr_0^2} + \int_{r_0}^{\infty} \frac{2f^{-1}(\tau)r_0^2}{Xr^3} dr \\ \text{prob}(t \leq \tau) &= \frac{f^{-1}(\tau)(9wf^{-1}(\tau) + 48r_0^2 - 4f^{-1}(\tau)^2 - 6w^2)}{24Xr_0^2}. \end{aligned} \quad (9)$$

When  $\frac{w}{2} \geq r_0$ , we shall examine two cases:  $r_0 \geq \frac{w-f^{-1}(\tau)}{2}$  and  $r_0 \leq \frac{w-f^{-1}(\tau)}{2}$ . Thus

$$\begin{aligned} \text{prob}(t \leq \tau \mid_{r_0 \geq \frac{w-f^{-1}(\tau)}{2}}) &= \int_{\frac{w-f^{-1}(\tau)}{2}}^{r_0} \frac{(2f^{-1}(\tau) + 2r - w)r}{Xr_0^2} dr + \\ &+ \int_{r_0}^{\frac{w}{2}} \frac{(2f^{-1}(\tau) + 2r - w)r_0^2}{Xr^3} dr + \int_{\frac{w}{2}}^{\infty} \frac{2f^{-1}(\tau)r_0^2}{Xr^3} dr \\ \text{prob}(t \leq \tau \mid_{r_0 \geq \frac{w-f^{-1}(\tau)}{2}}) &= \frac{64wr_0^3 + w^4 - 6w^3f^{-1}(\tau) + 9w^2(f^{-1}(\tau))^2}{24wXr_0^2} + \\ &+ \frac{48wf^{-1}(\tau)r_0^2 - 4w(f^{-1}(\tau))^3 - 24w^2r_0^2 - 48r_0^4}{24wXr_0^2}. \end{aligned} \quad (10)$$

$$\begin{aligned} \text{prob}(t \leq \tau \mid_{r_0 \leq \frac{w-f^{-1}(\tau)}{2}}) &= \int_{\frac{w-f^{-1}(\tau)}{2}}^{\frac{w}{2}} \frac{(2f^{-1}(\tau) + 2r - w)r_0^2}{Xr^3} dr + \int_{\frac{w}{2}}^{\infty} \frac{2f^{-1}(\tau)r_0^2}{Xr^3} dr \\ \text{prob}(t \leq \tau \mid_{r_0 \leq \frac{w-f^{-1}(\tau)}{2}}) &= \frac{2f^{-1}(\tau)r_0^2(2w - f^{-1}(\tau))}{wX(f^{-1}(\tau) - w)^2} \end{aligned} \quad (11)$$

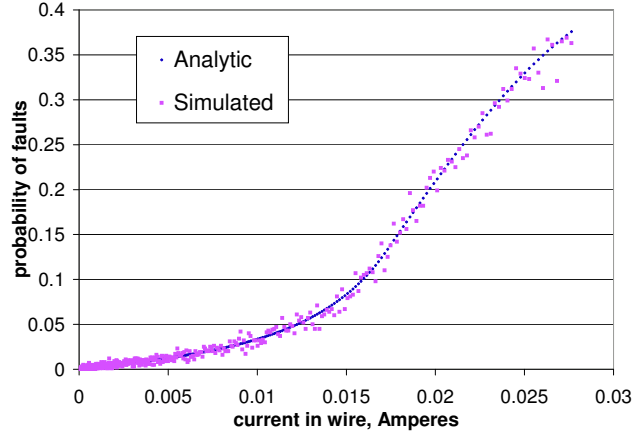
Summarizing the preceding results, note that Eq. 9, 10, and 11 refer to three different cases of relations between  $r_0$ ,  $\tau$ , and  $w$ . Also, recall that from Eq. 4,  $f^{-1}(\tau) = \sqrt[3]{\tau/C}$ .

All the above results have an apparent property: when the required width decreases towards zero, meaning the DC current in the wire is negligibly small, the average EP fault probability tends towards zero too. Indeed, Equations 9 and 11 have  $w_{req}$  as a factor in the numerator, causing the whole expression to go to zero. Equation 10, however, is not feasible under the assumption  $w_{req} \rightarrow 0$ , since its two conditions  $r_0 > \frac{w-w_{req}}{2} = \frac{w}{2}$  and  $\frac{w}{2} \geq r_0$  become contradictory.

Thereby, the EPY is more meaningful for nets with strong DC currents, such as power grid wires and analog circuits with strong bias current.

### 3 Simulations

Previous Section shows that even for very simple case, the analytical solution may be very complicated. Realistic design analysis, usually lacking periodicity, require simulation. EPYSIM simulator is our implementation of a tool that evaluate EPY for given small design. EPYSIM's key features:



**Figure 3. The simulated and analytically calculated MTTF-dependent parametric fault probability as a function of current in a single wire.**

- Employs Monte Carlo approach. Places a large number of defects with their radii distributed according to  $S(r)$  (Eq. 1), checks if a defect causes a parametric fault—notes the MTTF diminution. For given  $\text{MTTF} = t$ , EPY is the ratio between the number of defects, causing MTTF degradation below  $t$ , and the total number of defects.
- Uses (modified) “Mersenne Twister 19937” random generator.
- Written in C++, about 1500 code lines.

Figure 3 shows simulation and analytical results for the case discussed in Sec. 2. The graph shows quite a good matching of simulation results to analytical solution.

Getting the exact EPY for realistic chip would require considering many additional parameters, as spatial defects distribution, redundancy, process characterization, and more. There are tools for yield estimation that take these factors into consideration [4, 6]. On the other hand, in [9] shown that the number of reliability defects is proportional to the number of catastrophic defects:

$$\text{Reliability defects}^\dagger = k \cdot \text{Catastrophic defects} \quad (12)$$

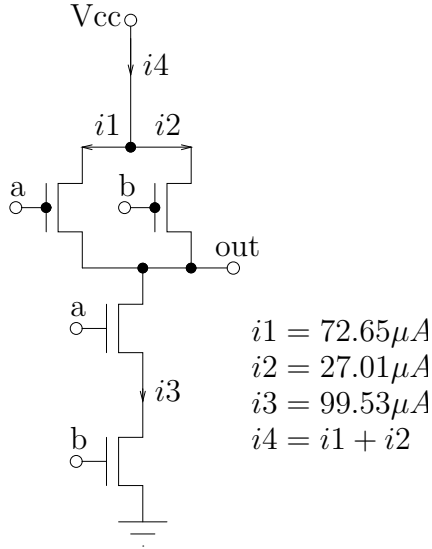
Thus we shall present the following results in terms of the *ratio between electromigration-dependent parametric faults and catastrophic faults*.

We shall present simulation results for a circuit built of 100 NAND2 gates. A single gate scheme and layout are shown in Fig. 4 and 5. Simulation time is 340 seconds on Pentium III 550MHz machine with 256MB of RAM for each temperature. Relying on the resulting graph in Fig. 6, we conclude the following corollaries:

1. For low temperature the ratio between EPY and catastrophic yield is between 0.002 at  $\text{MTTF} = 1$  year to 0.006 at  $\text{MTTF} = 20$  years, meaning that for process with 80% yield, 0.4 – 1.2 chips out of 1000 produced will fail in 20 years. This ratio is of good matching with [9], that propose  $k = 100 - 500$ , based on statistical data.
2. Working temperature has a huge effect on EPY. At temperatures above 400°K (126°C), which become more and more common in different applications, including analog and

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<sup>†</sup>Defects that cause early life (< 1 year) failures



**Figure 4. The NAND gate used for simulations and average DC currents in the branches. Only DC component of the current affects MTF due to electromigration, as described in [14].**



**Figure 5. The layout of the NAND2 gate. Only the first metal layer is shown.**

mixed designs, the ratio rises to 0.1 and even more. That means that for process with yield of 80%, operating at high temperature, 20 out of 1000 produced chips are supposed to fail in 20 years. This may have high importance in life-supporting, automotive, space and other applications.

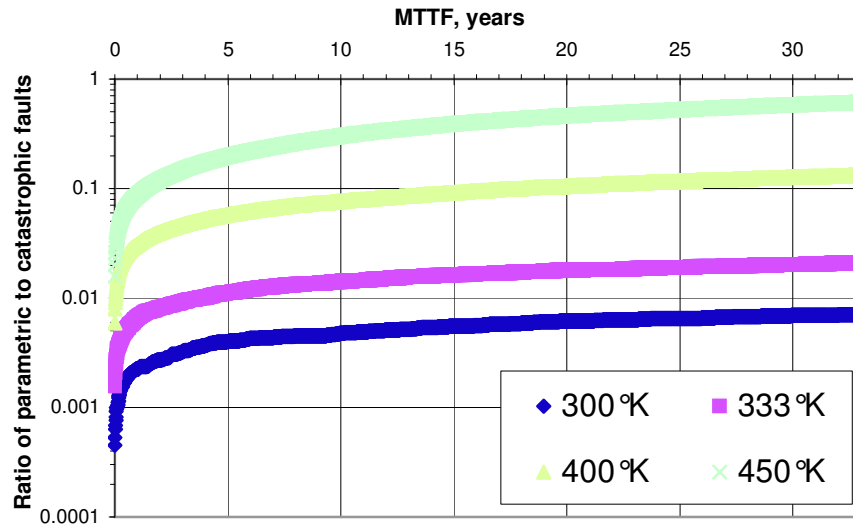
## 4 Summary

In this paper a new yield problem is defined: what is the measure of non-catastrophic chip faults due to electromigration as a result of defects at fabrication stage? Analysis was presented for a simple case of a single wire in the center of large die. The electromigration-dependent parametric fault probability of this pattern is a multicased expression that depends on about 10 parameters. A special simulation program — EPYSIM — was used to compare the analytical calculations with real defects, and to observe the EPY on more complicated patterns, as NAND gate array. We show that in some cases the EPY makes a significant contribution to yield estimation of VLSI chip.

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**Figure 6. The simulation of NAND gate presented in Fig. 4 under the temperature of 400°K. The graph shows that the effect of EPY may be large.**

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