

# 45nm Low Power CMOS Logic Compatible Embedded STT MRAM Utilizing a Reverse-Connection 1T/1MTJ Cell

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## Abstract

This paper reports a 45nm spin-transfer-torque (STT) MRAM embedded into a standard CMOS logic platform that employs low-power (LP) transistors and Cu/low-k BEOL. We believe that this is the first-ever demonstration of embedded STT MRAM that is fully compatible with the 45nm logic technology. To ensure the switching margin, a novel “reverse-connection” 1T/1MT cell has been developed with a cell size of 0.1026  $\mu\text{m}^2$ . This cell is utilized to build embedded memory macros up to 32 Mbits in density. Device attributes and design windows have been examined by considering PVT variations to secure operating margins. Promising early reliability data on endurance, read disturb, and thermal stability have been obtained.

## Introduction

STT MRAM has emerged as a potential next-generation NVM<sup>1-6</sup> with compelling advantages in scalability, speed, and energy consumption. While the attributes of STT MRAM are promising, particularly as an embedded memory for low-power mobile applications, there has been limited effort to demonstrate the technology in conjunction with an advanced logic technology. A primary challenge is integrating nano-scale magnetic tunnel junctions (MTJs) into advanced Cu/Low-K BEOL without disrupting the logic design rules and process modules. Furthermore, facilitating reliable read and write operations using deeply scaled LP FETs requires extensive efforts on tuning the MTJ physical, electrical, and magnetic attributes. In this work, we demonstrate for the first time a 45nm STT MRAM built on a standard CMOS LP logic platform.

## Results

The attributes of device characteristics applied for 45nm STT MRAM macros are described in Table 1. A primary challenge in constructing a cell embedded for LP applications is relatively small drive current ( $I_{\text{on}}$ ) pertaining to the LP NMOS access transistor. The current supplied to the MTJ ( $I_{\text{MTJ}}$ ) must be larger than the switching current threshold ( $I_c$ ). In general,  $I_c$  for the parallel (LRS) to antiparallel (HRS) state,

TABLE I  
Description of the 45nm embedded STT MRAM cell of this work

$V_{\text{DD}}$ (core/IO)	1.1 / 1.8V
Cell Architecture	Reversely connected 1T/1MTJ
Cell Size	0.1026 $\mu\text{m}^2$
Access NMOS (L/W)	40/270nm
MTJ Size	40nm (short axis)
MTJ Aspect Ratio	2.5~3
TMR/RA	110% / 9 ohm· $\mu\text{m}^2$
BEOL	Cu/Low-K, 7 metal layers

$I_c(P \rightarrow AP)$ , is 20~50% larger than  $I_c(AP \rightarrow P)$ . Furthermore, the common 1T/1MTJ architecture shown in Fig. 1(a) suffers from a severe “source degeneration” effect for the  $P \rightarrow AP$  switching, causing  $I_{\text{MTJ}}(P \rightarrow AP)$  significantly smaller than  $I_{\text{MTJ}}(AP \rightarrow P)$ . Coupling these two, the  $P \rightarrow AP$  switching is difficult to achieve for the conventional cell. To mitigate this problem, we have developed a reversely connected 1T/1MTJ cell as shown in Fig. 1(b), for which the source-degeneration effect influences only the less demanding  $AP \rightarrow P$  switching. The advantage of our novel cell is illustrated in Fig. 2. The switching loop measured at 100ns is fully contained within the available range of  $V_{\text{MTJ}}$  and  $I_{\text{MTJ}}$  while the  $P \rightarrow AP$  switching cannot be realized for the conventional cell.

The memory array architecture built on the reverse-connection cell is shown in Fig. 3 with the relevant biasing conditions to program LRS (“0”). The word line (WL) may be overdriven, while both the bit line (BL) and the source line (SL) remain at  $V_{\text{DD}}$ . Since WL is activated dynamically only for the span of fast read and write (<100ns), such overdrive is acceptable without sacrificing the reliability criteria. Using this array architecture, we designed fully-featured memory macros up to 32Mbits in density, as shown in Fig. 4. A cross-sectional TEM photo of the die and a planar SEM photo of a representative MTJ are shown in Fig. 5. The MTJ is integrated

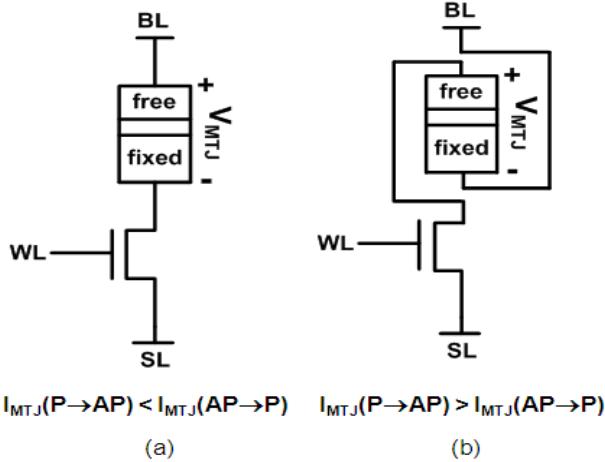


Fig. 1: STT MRAM cell architecture comparison: (a) conventional cell (b) reverse-connection cell developed in this work. For the reverse-connection cell,  $I_{MTJ}$  is larger for the  $P \rightarrow AP$  switching which alleviates the effect of the  $I_c$  asymmetry ( $I_c(P \rightarrow AP)/I_c(AP \rightarrow P) > 1$ ).

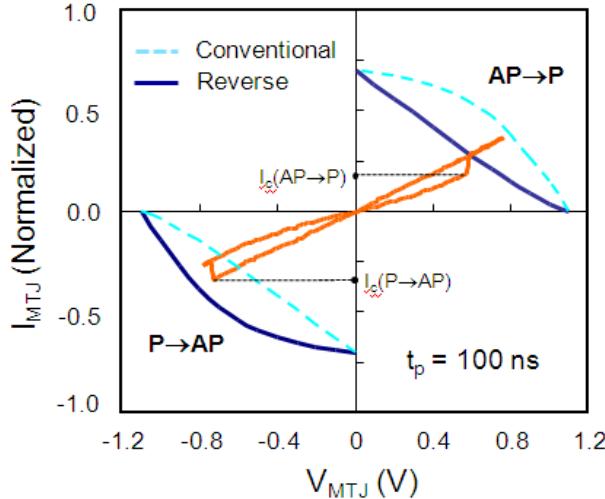


Fig. 2: Loadline analysis for the MTJ switching loop (measured using a 100ns pulse) that illustrates an improvement in switching margin with the reverse-connection cell. For switching to occur,  $I_{MTJ}$  must be larger than  $I_c$  (switching current threshold). For the conventional cell in this example, the  $P \rightarrow AP$  switching cannot be realized.

between M3 and M4 by utilizing a state-of-the-art 300mm-wafer MRAM modules. The MTJ has been fabricated by PVD (except the MgO barrier by oxidation) and RIE.

To ensure read and write margins along with the reliability against MTJ breakdown, both  $\Delta_1$  and  $\Delta_2$  in Fig. 6 must be secured after considering all the parametric variations at PVT corners. As illustrated in Fig. 7, a challenge is to deal with a variety of MTJ physical and operating parameters which are coupled with one another. We have developed a statistical methodology to account for the variables and to find an optimum design window. As shown in Fig. 8, nine parameters

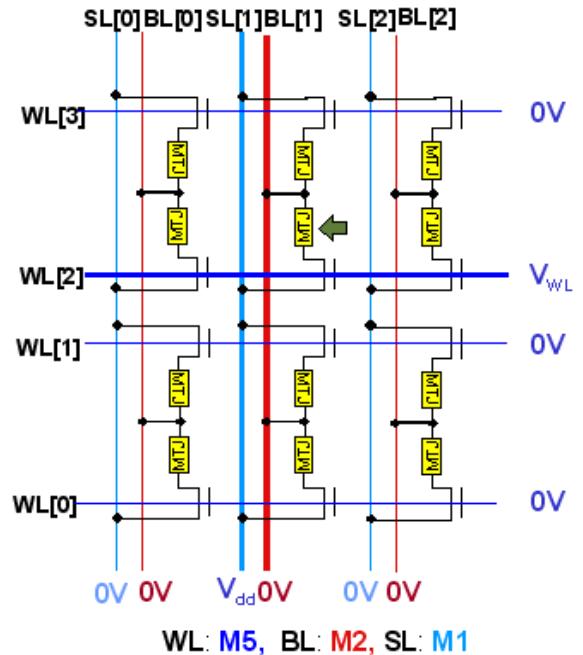


Fig. 3: Array architecture and an example of the LRS (low resistance state) programming condition ( $AP \rightarrow P$  switching) for the cell marked by the arrow. WL, BL, and SL represent word line, bit line, and source line, respectively.

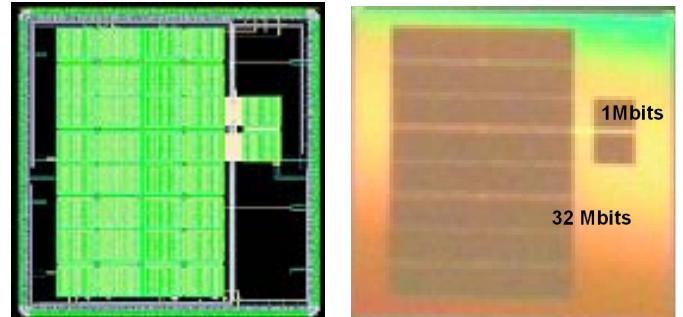


Fig. 4: A die photo showing two fully featured macros: 32 Mbit and 1 Mbit in density, respectively.

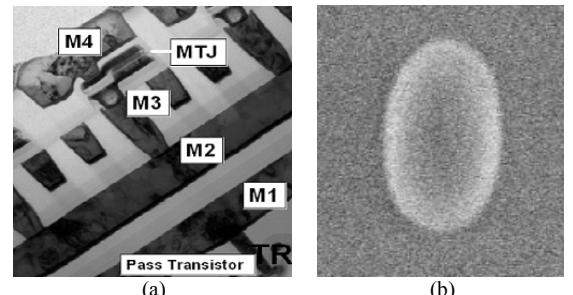


Fig. 5: (a) cross-sectional TEM view of the embedded STT MRAM die. The MTJ is integrated between M3 and M4. The photo shows the metal level up to M4 while the chip has 7 layers of metals; (b) a planar SEM photo of an MTJ.

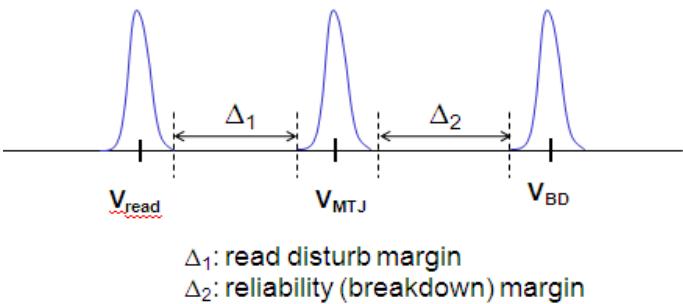


Fig. 6: A schematic description of finding a design window in terms of MTJ read, write, and breakdown voltage distributions.

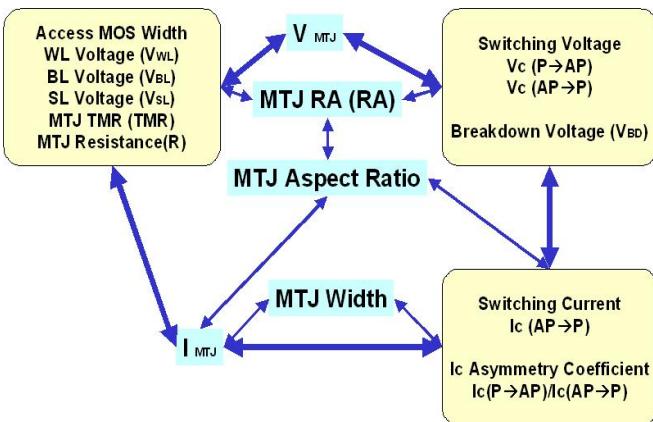


Fig. 7: Correlations of cell design parameters that must be optimized to meet the conditions in Figs. 2, 3, and 6.

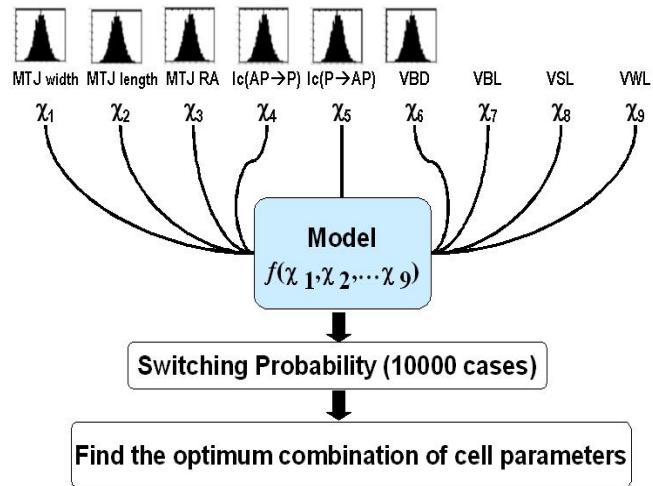


Fig. 8: Variation-aware statistical device-design methodology is developed for this work to ensure secure operation and reliability windows. Relatively wide parametric variations at this stage of 45nm embedded STT MRAM development are often related to controlling MTJ resistance and area distributions. This work has considered the MTJ RA (resistance-area product) distribution of  $\pm 3\sigma$  for circuit and macro simulations.

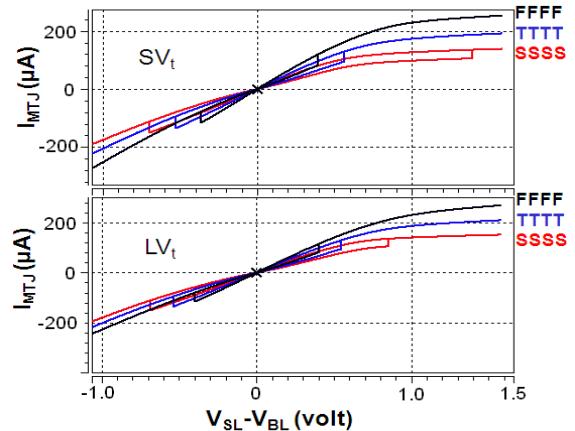


Fig. 9: Switching windows with all PVT corners considered. To secure switching at the “worst-case” (SSSS) write condition, the SVt case needs  $V_{SL}$  overdrive. The LVt case has an adequate margin without an SL or BL overdrive.

and their statistical variations are analyzed for 10,000 cells to ensure the design window. Utilizing this methodology, embedded STT MRAM macros can be designed securely by meeting the requirements shown in Table 1, Figs. 2, 3, and 6. This methodology has led us to develop two access transistor  $V_t$  flavors whose switching windows are shown in Fig. 9.

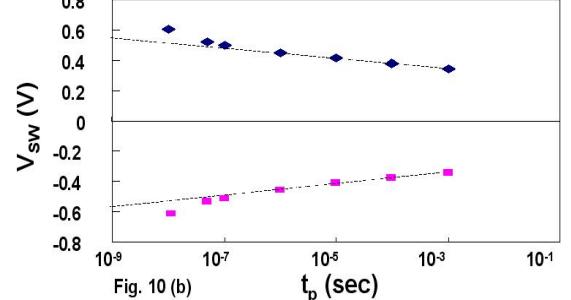
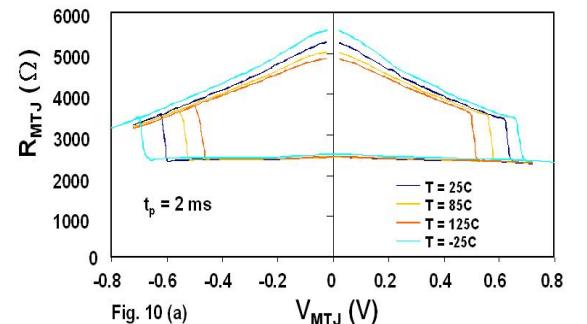


Fig. 10: (a) The switching characteristics measured as a function of temperature, and (b) as a function of pulse width down to 10ns.

The device switching characteristics measured as a function of temperature (-25~125°C) and a pulse width (10ns~1ms) are plotted in Fig. 10(a) and (b), respectively. The RH hysteresis curve of a selective MTJ is shown in Fig. 11(a). The energy barrier (thermal stability) estimated from Fig. 11(b) is 51 k<sub>B</sub>T. Though not too small for such deeply scaled MTJs, we expect the energy barrier to increase as our MTJ process further matures. Early results on endurance and read disturb are shown in Fig. 12, which demonstrate the promising nature of STT MRAM reliability as an embedded NVM.

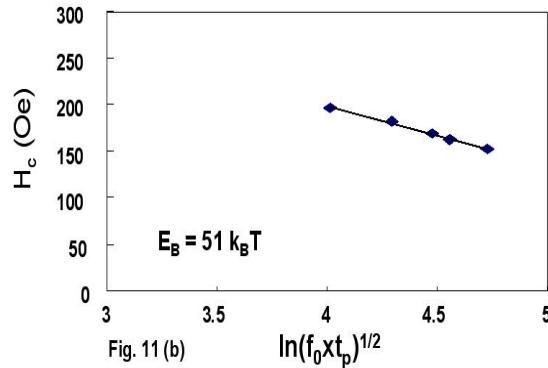
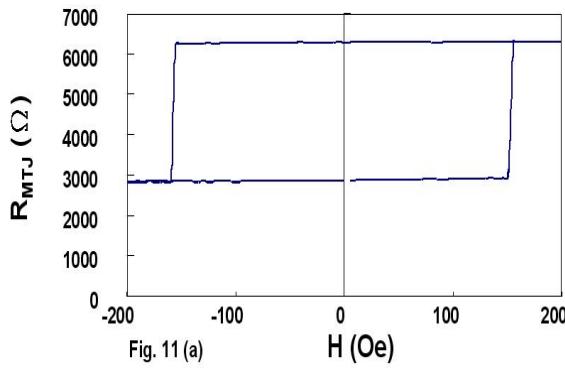


Fig. 11: (a) MTJ RH loop and (b) energy barrier estimation

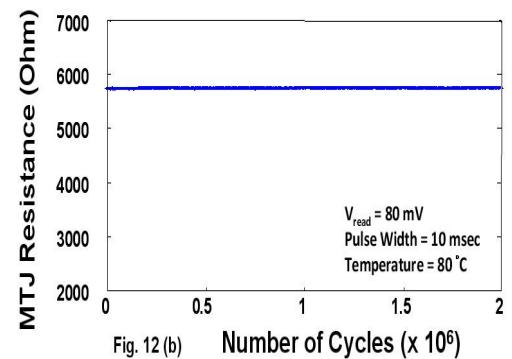
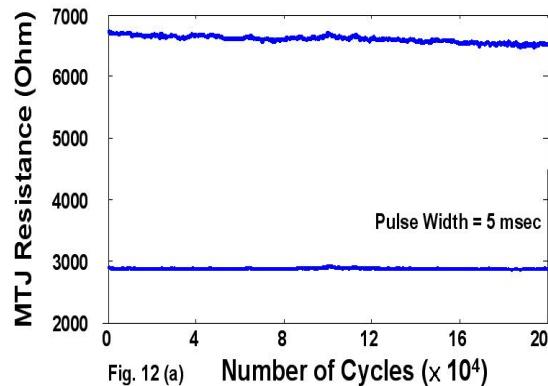


Fig. 12: (a) Endurance test under  $2 \times 10^5$  cycles of 5 ms pulses (equivalent to  $10^{11}$  cycles of 10 ns pulses, Ref. 6), and (b) Read disturb test under  $2 \times 10^6$  cycles of 10 msec and 80 mV (equivalent to  $2 \times 10^{12}$  cycles of 10 ns pulses).

## Summary

We have demonstrated, for the first time, a 45nm embedded STT MRAM fully compatible with a standard CMOS logic platform that employs LP transistors and Cu/Low-K BEOL. We have developed the reverse-connection 1T/1MTJ cell and the statistical design methodology to secure operating margins. The results of this work suggest that STT MRAM can be enabled as an attractive nonvolatile embedded memory for advanced LP logic technologies.

## References

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